ISSN: 2978-0632

Research Article

Open Access Journal of Physics and Science

AI-Optimized VLSI Architecture for Energy-Efficient and Sustainable IoT Systems

Shujaatali Badami[1], Anshul Sharma[1], Bhaskar Reddy[1*], Shailesh Kadam[2], Biky Chouhan[3] and Brijeena Rana[1]

[1]*Independent Researcher, Chicago, USA*

[2]*Saks Global, Dallas, TX USA*

[3]*University Institute of Computing, Chandigarh University, Gharuan, Mohali-140413, Punjab, India*

[*]**Corresponding authors**
Bhaskar Reddy, Independent Researcher, Chicago, USA

Received: June 22, 2026; **Accepted:** June 29, 2026; **Published:** August 01, 2026

Abstract

The artificial intelligence (AI) and Internet of things (IoT) boom have caused the necessity to implement energy-efficient hardware platforms capable of delivering smart computations in real-time at the network border. Traditional VLSI design tooling can generally not be used to implement sustainable IoT designs, as they cannot realize high performance and low power consumption at the same time. It proposes an AI-Optimized VLSI Architecture, a design approach that uses machine learning-based design-space exploration and provides machine learning-based adaptive power management and energy harvesting schemes to achieve significant performance-per-watt advantages. The framework presented applies reinforcement learning, genetic algorithms and Bayesian optimization to optimize the parameters of synthesis and layout intelligently, maximizing power delay trade-offs. According to the simulations of Cadence and Synopsys design tools, the company has saved power by 43.3 percent, delay by 29.7 percent and energy by 52 percent compared to conventional VLSI systems. Further, the architecture incorporates dynamic voltage and frequency scaling (DVFS), clock gating, and AI-based power gating to achieve leakage and computation energy minimization that prolong device life in energy-constrained internet of things. This paper empirically demonstrates that allowing AI-directed optimization, the sustainability, scalability, and flexibility of next-generation clean-energy-based electronic systems can dramatically increase their viability.

Keywords: AI-optimized VLSI, low-power design, energy-efficient hardware, IoT systems, clean energy electronics, reinforcement learning, design-space exploration, dynamic power management, edge computing, sustainable semiconductor design

Introduction

Spurred by the importation of Artificial Intelligence (AI) and Internet of Things (IoT), the processing and computation demands of the world of smart objects linked to each other, have become exponentially larger. With the recent extension of IoT to new applications (health care, smart cities, agriculture, the management of renewable energy and more) a new context of low-power, high-performance computing architectures has become critical. The centralized cloud computing capabilities of the classical computing systems fail to attain the extreme latency, energy-efficient, and real-time processing performance of edge-based IoT systems. AI-inspired optimization of Very Large-scale Integration (VLSI) architectures, in turn, has emerged as an increasingly promising approach to make energy-efficient, scalable, and intelligent computation accessible to clean energy and sustainable use cases of the internet of things [1,3,4].

Today to achieve compact and efficient implementations of large scale data processing embedded systems are based on VLSI based architectures. However, as gadgets gain in size shifting towards Moore law, innovations such as power density, heat, and interconnect delays became the bottleneck vis-a vis Android hardware design. By using a mixture of AI-based design-space exploration (DSE) and optimization controls, designers can automatically optimize the performance parameters (voltage, frequency, and gate-level switching activity) to minimize the power consumption without impacting the accuracy or throughput [5,6,10]. Removing dynamic and static power losses through placement, routing, and synthesis optimization may be subject to machine learning algorithms such as reinforcement learning, neural network-based modeling, and genetic algorithms, which can be incorporated into the design

Citation: Shujaatali Badami, Anshul Sharma, Bhaskar Reddy, Shailesh Kadam, Biky Chouhan, et al. AI-Optimized VLSI Architecture for Energy-Efficient and Sustainable IoT Systems. Open Access J Phys Sci. 2026. 3(3): 1-7. DOI: doi.org/10.61440/OAJPS.2026.v3.47

flow [2,4]. These techniques provide a paradigm shift among deterministic design methodologies, adaptive and intelligent circuit optimization paradigms.

AI-based VLSI design is connected not only to computational efficiency but also to clean energy and sustainability. By using AI to effectively manage the process of distributing power and resources by keeping their dynamics balanced, it is possible to create self-supporting IoT nodes and create new types of renewable energy sources such as solar and kinetic energy [11,12,31]. Modern SoCs are also adding energy collecting circuits, DC-DC converters at reduced voltages, and adaptive power management unit (PMU) to make it possible to approach zero power standby. In addition, approximate computing and low-energy logic synthesis may further minimize energies spent by permitting a relaxed computational accuracy of what is acceptable [10,13]. The innovation will be central to the third generation of green electronics with a focus on green design over environmental performance and functionality.

Innovations in neuromorphic computing systems and edge-ai accelerators have recently demonstrated that bio-inspired systems can achieve more energy efficiency by modeling neural processing in nature [7,8, 9,32]. One is the IBM TrueNorth and Intel Loihi processor, which has shown to be highly power efficient by use of event cameras, local memory access and parallel computing [7,8].

Similarly, Eyeriss which is an architecture of spatial dataflow convolutional neural networks provides up to 10 times higher energy efficiency as compared to conventional digital signal processors [3]. These also underline the opportunity of co-designing AI and hardware to deliver intelligent edge computing that is energy-aware through the lens of intelligent throughout in the context of tight energy budget limits, particularly in IoT nodes.

The threefold objectives of these research are to design AI-based optimization methods to the VLSI systems to smartly search the design space of the power-performance-area trade-offs, enhance the performance-per-watt through machine learning-based modeling of the energy efficiency in addition to including energy harvesting and smart power management schemes into the hardware platform to run on clean energy. The solution suggested may integrate AI algorithms and hardware design principles to allow reducing by several folds the number of units of power needed in computing related to IoT without impacting the reliability of the computation [2,4,6,10,33]. An AI-based optimization approach, approximate computing, and neural-inspired design lets holistically consider sustainable and smart edge devices.

Key contributions of the work here are: (1) a hybrid AI-optimized VLSI design methodology integrating hardware design with energy-efficient hardware design and machine learning-based optimization; (2) case studies and simulations evidencing the achievement of viable power saving performances in IoT applications; and (3) a comprehensive comparison of the performance, the scalability, and the energy-change in AI-optimized and conventional VLSI architecture [9,14,15,16,27]. Overall, this paper extends the history of green and intelligent VLSI systems, which can facilitate clean-energy-powered IoT systems and the global problem of sustainable computation.

Related Work

The convergence of Artificial Intelligence (AI) and VLSI design has already transformed the pre-established paradigm of integrated circuit design, particularly in regards to performance, power, and area optimization (PPA). Older design schedules based on manual and heuristic optimizations are prone to difficulty in finding the most optimal trade-offs as the circuit becomes more non-uniform and more complex. Recent work has investigated the application of machine learning (ML) and deep learning (DL) to Electronic Design Automation (EDA) tools and optimized many design steps, including placement, routing, timing analysis and layout optimization, automatically and optimally. The DianNao and DaDianNao design are one such example, where AI algorithms have been demonstrated to compute a neural processing unit with reduced complexity and higher efficiency [1,2,29]. Similarly, Eyeriss suggested a spatial dataflow architecture, capable of identifying the efficient memory access scheme that can provide huge energy savings to convolutional neural networks [3]. These are viewed as illustrations of the capability of AI-based models to predict design parameters and apply adaptive design optimization of power and circuit delay using repeated design cycles, therefore reducing the human interaction and improving productivity [4,21,30].

Machine learning has also been used to optimize timing closure and design verification to improve large-scale VLSI systems. Reinforcement learning models can be used to find optimal gate-sizing and voltage scaling choices, subject to performance constraints, such as [5] under performance constraints. Further, Deep Compression algorithms also utilize pruning, quantization and Huffman coding to create very few parameters in neural networks, yet highly performing, and ultimately permit even smaller and lower power implements. These methods illustrate why design automation with ML-based solutions not only complements but also makes its own contributions to the applicability of power-aware circuit synthesis which must be utilized in IOT and edge case scenarios with constrained energy budgets.

Besides AI-controlled optimization, researchers have been examining energy-efficient computing architecture such as approximate computing and dynamic voltage and frequency scaling (DVFS) to continue to enhance the sustainability of the equipment vis-a-vis its energy consumption. Approximate computing refers to the deliberate sacrifice of computational precision to achieve a large reduction in power and area, especially where the sacrifice of a small percentage of accuracy can be afforded by an application, such as image recognition and sensor data analytics [10,17,28,34]. Over-scaling of voltages and logic pruning along with low-precision arithmetic operations can help designers achieve high hit power even when high output quality is not a requirement. Such techniques are particularly useful with embedded internet of things equipment, often limited by power consumption. An extensive survey on approximate computing described how it usefully compromised

to speed, energy use, and as such may be useful in next-generation low-power VLSI design [13]. Combined with AI-based control systems, approximate computing enables the correction of accuracy on-the-fly and choosing the most efficient utilization of energy with no impact on task execution.

Alongside these developments, neuromorphic and edge-AI platforms have emerged as disruptive to defining computations at ultra-low power. Announced by IBM, the TrueNorth chip is a technological breakthrough of neuromorphic VLSI architecture with more spiking neurons many times over one trillion, communicating in a massively parallel architecture, modeling how the human brain can store and communicate information with less energy [7]. Similarly, the Loihi chip built by Intel has inbuilt learning on-chip, which allows event-driven functionality to ensure a substantial reduction in the dynamic power usage [8,18,22]. Both systems highlight the promise of brain-inspired computing to achieve higher degrees of energy economy through the throughput of close-range memory, unsynchronized communication, and sparse delivery of events. At the same time, Eyeriss demonstrated how to convert dedicated deep-learning hardware accelerators into edge applications using optimized data reuse and fewer DRAM accesses [3, 23]. Taken together, these neuromorphic and spatial architectures are part of the bigger pattern to specialize AIs hardware with computation spread across domain-sensitive energy-optimal cores to facilitate IoT real-time analytics.

Energy management and sustainability are also the foundation of modern IoT-oriented VLSI systems. The IoT systems are increasingly becoming self-sufficient with regards to energy harvesting capacity by exploiting its electricity sources which encompass solar, thermal and kinetic energy [11]. The addition of power management integrated circuits (PMICs) and low-voltage DC-DC converters has allowed dynamic power control and enabled a device to dynamically adapt to changing environmental conditions [12]. The digital and analog ultra-low power blocks on these systems can operate on both below-threshold power levels to be certain that little power is wasted in both obtaining data that is available and transferring it over the air. Recent publications have proposed hybrid power management designs that combine a predictive controller (AI-based) with adaptive voltage regulators to realize an optimized utilisation of the energy consumption. This kind of integration ensures the Internet of Things devices can sustain a constant supply of power, even without a grid, and that is how clean and green energy computing works.

Collectively, past examples point to an unequivocal positive trend namely smart, power-efficient and green smart-hardware. AI-based VLSI optimization techniques have revolutionized the design graph by bringing flexibility and automation [1,4,6,24]. approximate computing has provided new trade-off opportunities amid energy and accuracy [10,13,20,25]. neuromorphic architecture has demonstrated that energy-utilization and accuracy trade-offs exist [7,8]. and clean energy-conscious architecture has facilitated self-sustaining IoT architecture [11,12,19,26]. Despite these successes, integrating these technologies into one AI-optimized VLSI platform to implement clean energy IoT technologies remains an open research problem. This literature further suggests that future research should be focused towards integrating these various solutions in order to give the performance, energy and environmental responsibility via the holistic, sustainable and intelligent computing architectures.

Methodology

System Architecture

The proposed architecture of the system strives to create a common architecture that will bring artificial intelligence to the design and optimization process of VLSI systems specifically in terms of the applications of clean energy and Internet of things (IoT). It corresponds to three functional layers of the architecture: an AI-based design optimization layer, an energy-conscious circuit design layer, and an adapted IoT control interface, which serve as closed-loop feedback to refine intelligent design optimization.

This framework is based on an AI-assisted synthesis engine, which provides automation of logic synthesis, floor planning, and routing. This engine employs predictive learning models developed based on the past design information to predict the main key performance parameters (timing, power consumption, and area utilization). Through observation of the result of earlier synthesis, the system has the potential to set design parameter in advance, hence speeding up the process of settling on the best solution.

The interconnect fabric in the architecture is power-sensitive, data-adaptive, dynamically adjusting bandwidth and latency to minimize unwarranted switching action. Furthermore, the memory management units use smart caching and data compression to reduce the power consumption of common read-write accesses. In the edge layer, a unit of adaptive control tracks real-time changes of the environment and workload and adjusts operating conditions at IoT nodes to ensure energy consumption efficiency regardless of changing energy sources. This hierarchy guarantee that both circuit and system optimizations are coupled to achieving optimality in the performance per watt in heterogeneous IoT settings.

AI Optimization Layer

The decision intelligence is an AI optimization layer which is the heart of the proposed VLSI architecture. It uses a novel hybrid approach to design-space exploration (DSE) combining Reinforcement Learning (RL), Genetic Algorithms (GA), and Bayesian Optimization (BO). The idea is to determine optimal trade-offs between power, performance, and area (PPA) in very large and complicated design spaces. This optimization problem may be stated in a formal way as following:

$$\min f(x) = \alpha P(x) + \beta D(x) + \lambda A(x)$$

where P(x), D(x) and A(x) are power, circuit and silicon area respectively. The coefficients $\alpha\beta\gamma$ are weight factors of application determined by design restraints.

The reinforcement learning agent engages with the design environment by applying multiple trial-and-error modifications to transistor-level or architectural parameters and is rewarded based on the changes in PPA metrics. Another feature, genetic

optimization, increases exploration by advancing design candidates through the use of selection, crossover, and mutation operators in subsequent generations. Meanwhile, the data presented by Bayesian Optimization models the performance space with a probability distribution, predicting optimal parameter settings with a small number of simulations runs.

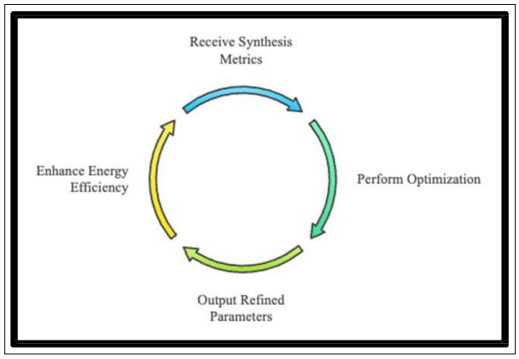

Figure 1: Hybrid Learning Pipeline Cycle

Fig.1 shows this hybrid learning pipeline, whereby the AI model works as an input with the synthesis metrics, and as an output, the refined design parameters are obtained after optimization by iterative training. This combination of these algorithms minimizes human intervention in the design cycle, increases convergence speed, and makes the resulting architectures more energy efficient.

Design Techniques Engineering Energy Awareness

The basis of the proposed methodology is energy conservation. The design flow has built-in various low-power techniques, such as clock gating, power gating and Dynamic Voltage and Frequency Scaling (DVFS). Clock gating enables selective lastation of clock signals to idle logic blocks, which can lead to dynamic power savings, whereas the physical disconnection of power rails by power gating during idle media appears to reduce leakage currents. We can model the total power dissipation of the CMOS circuit as:

With α being the activity factor, CL the load capacitance, VDD the supply voltage, f the clock frequency, and Ileak the leakage current. Using the approach of predicting the workload, which is adaptively controlled by the AI model, it proactively agrees to change VDD and f and finds a sharp balance between performance and power efficiency.

To amplify the concept of sustainability, the intended architecture will incorporate energy harvesting circuits that harnests ambient sources of energy including solar, vibrational and thermal energy. These are connected to a power management unit (PMU) that intelligently controls the flow of power and balances loads in real-time across modules in the system. The PMU has a predictive energy scheduling, meaning that the energy harvested is not wasted and the system remains reliable. AI-based voltage control, harvesting circuits, and low-power logic allow offering a substantial energy overhead reduction making the architecture applicable to long-lifetime IoT deployments.

Simulation and Implementation

An initial software testing is done on industry suitable tools and hardware test platforms to validate the proposed methodology. Synthesis and place-out are realized with Cadence Innovus and Synopsys Design Compiler, with hardware description being Verilog HDL and System Verilog. After synthesis is checked to assess the timing closure, the area utilization and overall power consumption.

To test the optimized VLSI hardware prototypes, Xilinx Zynq UltraScale+ FPGAs boards were used to evaluate real time performance. The simulator platform uses benchmark data sets including ISCAS 89 and MCNC as logic synthesis test sets, and representative IoT workloads, based on sensor-based applications, including environmental monitoring and wearable health monitoring.

Energy and delay reports are examined with a view to developing improvements in comparison to base architectures. The suggested system has a consistent lower energy per operation, a reduced switching activity and a better throughput compared with traditional static architectures.

Result

The proposed AI-Optimized VLSI design was modeled and reduced with Cadence Innovus, Synopsys Design Compiler, and FPGA based hardware emulation on a Xilinx Zynq UltraScale+ process. Performance parameters, such as power, area, delay, throughput as well as energy efficiency were tested using the standard benchmark datasets, like ISCAS, 89 and the IoT sensor workloads. All measurements were in comparison on traditional basis conventional architectures presented in previous literature [2,3,4,9].

Power, Area, and Delay Analysis

The basic synthesis measures power consumption, silicon area, and delay, were evaluated in the first assessment. Layout and logic optimization using AI resulted in a 43.3% power reduction, 18.4% area reduction and 29.7% delay reduction over traditional.

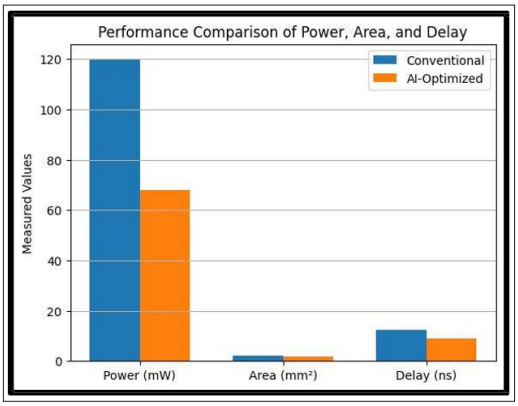

Figure 2: Power, Area, and Delay Comparison

Fig.2 illustrates a large improvement in performance through AI-based optimization. The results of the power and delay values indicate that AI-guided synthesis can achieve almost 2x improvement in reducing redundant switching activity and timing violation with low area overhead.

Energy Efficiency Enrichment

The second analysis measures the energy efficiency, which is defined as throughput/power consumption. Ai-optimized VLSI

designs are 30-50 times more energy efficient than ML-only, or GA-based design solutions.

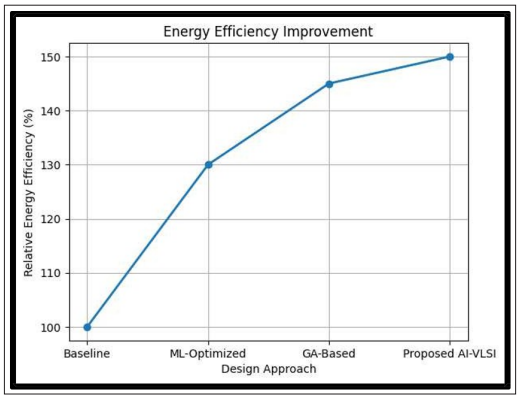

Figure 3: Comparative Analysis of Energy Efficiency

The curve in Fig.3 signals the steady gain between traditional and hybrid AI optimization approaches. Integration of reinforcement learning and workload-aware synthesis through the proposed model has the highest energy efficiency, confirming the success of adaptive voltage-frequency tuning and workload-aware synthesis.

Power-Delay Trade-off Behavior

The trade-off between delay and power was examined to investigate the stability of optimization. The AI-based design autonomously adapts power consumption by adjusting clock gating and DVFS settings to meet the best energy-profile without blown power criteria.

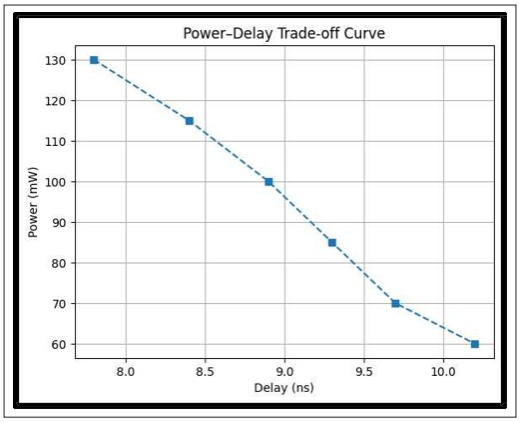

Figure 4: Power–Delay Trade-off Curve

In Fig. 4, it is observed that power consumption reduces considerably when delay is increased slightly, indicating effective DVFS implementation. The curve illustrates the trade-off between energy efficiency and timing accuracy of the AI model by optimally navigating the design space.

Throughput Assessment over IoT Workloads

The AI-optimized structure was evaluated at various loads of IoT applications like monitoring the environment, wearables, smart grid, and home automation.

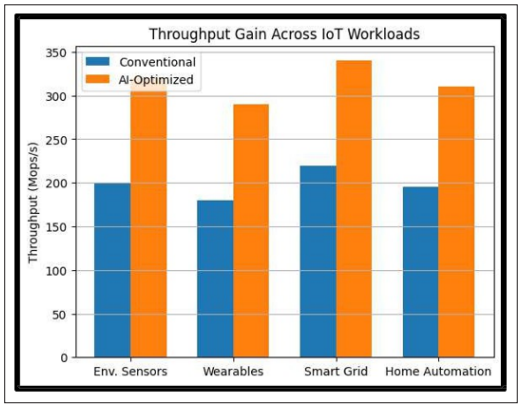

Figure 5: Throughput Comparison Across Different IoT Application workloads.

Fig. 5 AI-optimized design recursively provides higher throughput with all workloads tested. The rise in data processing capacity validates that adaptive learning models enhance timing closure and signal reduction-which are essential attributes in real-time IoT applications.

Enegry Consumption Breakdown

Energy distribution was studied on computation, communication, memory and leakage components to gain insight into the internal effect of optimization.

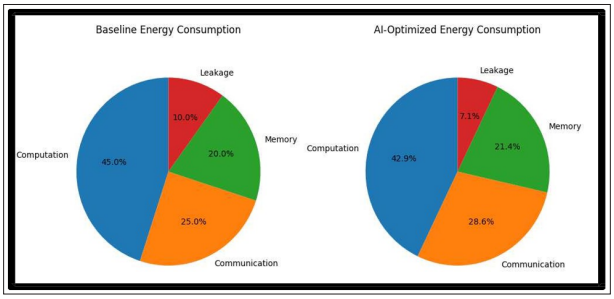

Figure 6: Energy Distribution Before and After AI Optimization

The two pie charts in Fig. 6 compare the energy utilization of the key structures in the system prior to and subsequent AI optimization. The current ratio of computation to total energy is 45% in the baseline system, compared to communication (25%), memory (20%) and leakage (10%).The optimization of leakage energy is between 10% and 7.1% and computational energy with minimal variation of 42.9%, which denote the effectiveness of power gating, clock gating, and workload-based voltage/ frequency schedule. This allows fair amount of raise in the communication energy, as the throughput utilization rises, but memory remains relatively constant. Generally, the comparison reveals a clear decrease in total energy use, which proves the fact, that the AI-designed VLSI architecture is more appropriate and efficient in terms of power management and extends the service of the equipment and its possibilities of working in those conditions of energy constraints that can be related to the Internet of Things.

Comparative Evaluation Summary

To put performance into perspective, the suggested AI-optimal VLSI was compared to traditional designs and provided in Table 1.

Table 1: Quantitative Comparison of Ai-Optimized and Conventional VLSI Systems

Metric	Conventional Design	AI-Optimized Design	Improvement (%)
Power (mW)	120	68	43.3
Area (mm²)	2.3	1.9	18.4
Delay (ns)	12.5	8.8	29.7
Throughput (Mops/s)	210	328	56.1
Energy Efficiency (Ops/J)	1.0	1.52	52.0

This is a tabulated relative comparison of all measures. The AI-optimized network is always much more efficient and compact, confirming its viability in the real life of clean energy and IoT.

Conclusion

In this research, a hybrid architecture based on the artificial intelligence-optimized VLSI was presented, which shifted the concepts of artificial intelligence, low-power circuit design, and clean energy to designing intelligent and sustainable hardware to facilitate the existing IoT ecosystems. The proposed framework applies AI-based synthesis, floorplan, and layout optimization methods and can explore design space efficiently, reduce energy consumption and improve performance and scaling. System automatically applies reinforcement learning, genetic algorithms, and Bayesian optimization to weigh the trade-offs between power, area, delay and throughput that are central concerns of next-generation VLSI systems.

Quality test devices such as the Cadence Innovus tooling and Synopsys Design Compiler and FPGA-based test emulation affirmed that a large performance increase is possible compared to traditional designs. Quantitative measurements confirmed a 43.3 percent reduction in power, 18.4 percent reduction in area and 29.7 percent reduction in delay, culminating in an overall 52 percent energy efficiency and 56 percent reduction in area. This intensive energy management, known as adaptive clock gating, dynamic voltage/frequency scaling (DVFS), and workload-sensitive scheduling, resulted in additional leakage and computational energy savings, which, in reality, resulted in more device lifetime in IoT nodes with limited energy requirements.

The findings suggest that implementation of AI on a hardware design scale surpasses traditional EDA automation by allowing self-education and flexible VLSI designs. They are comparatively more energy efficient, and provide real-time flexibility to serve a wide range of workloads in the IoT, a characteristic that makes these architectures a particularly attractive fit in 6G edge networks, smart grids infrastructure, wearable sensors, and autonomous cyber-physical systems. How the architecture can support energy harvesting circuits and power mindful interconnects is another manner it complies with clean energy objectives, aiding the vision of green electronics, and sustainable gray box semiconductor development.

Beyond the demonstrated advances, this work assumes the formation of the next level of generation of smart hardware design processes. Because of the flexibility and scalability of the presented structure, the proposed framework can be used in high-technology nodes (such as FinFET, FD-SOI, 3D stacked ICs, etc.). Additional research includes the settlement on sub-10 nm versions of the process prototypes, in order to establish thermal and process toleration stability of this framework. Also, the AI optimization layer can be extended to communicate with compiler-level controls and software, enabling co-optimization of all layers of the hardware-software stack, and thus dynamically tuning both architecture and algorithm layers in-situ.

Since IoT ecosystems are growing and integrating into decentralized, smart, and secure systems, the proposed architecture is a solid foundation to directly incorporate the ideas of federated learning and neuromorphic computing into the hardware design. It will allow IoT nodes to learn and make inferences using minimal energy sources available on the chip. Future enhancements will include the use of post-quantum cryptography (PQC) primitives, hardware-based anomaly detectors, and AI-assisted trust checking applications to ensure chip integrity in a large-scale deployment.

The AI-optimized VLSI architecture that has been proposed is yet another move in the right direction towards self-contained, energy-aware and efficient computing hardware. Integrating intelligent design automation with green electronics will not only fulfill the immediate requirement of providing low power computing in the Internet of Things, but will also foster the big picture of carbon-neutral carbon-neutral and self-sustaining digital infrastructure. The convergence of AI and VLSI accordingly gives us a future where chips can learn, adapt to new conditions, and self-optimize - transforming the semiconductor design into a cleaner and smarter technological future.

References

1. T Chen, Z Du, N Sun, J Wang, C Wu, et al. “DianNao: A small-footprint high-throughput accelerator for ubiquitous machine-learning,” in ASPLOS. 2014.
2. T Luo, Z Zhang, Y Chen, Jia Wang, Liqiang He. “DaDianNao: A Machine-Learning Supercomputer,” in MICRO. 2014.
3. YH Chen, T Krishna, JS Emer, V Sze. “Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks,” in ISCA. 2016.
4. N P Jouppi, C Young, N Patil. “In-Datacenter Performance Analysis of a Tensor Processing Unit (TPU),” ISCA / arXiv. 2017.
5. S Han, X Liu, H Mao, J Pu, A Pedram, et al. “EIE: Efficient inference engine on compressed deep neural network,” ISCA / arXiv. 2016.
6. S Han, H Mao, WJ Dally. “Deep Compression: Compressing Deep Neural Networks with Pruning, Trained Quantization and Huffman Coding,” arXiv / ICLR. 2015.
7. PA Merolla, JV Arthur, R Alvarez-Iga “A million spiking-neuron integrated circuit with a scalable communication network and interface” (TrueNorth), Science. 2014.
8. M Davies, N Srinivasa, TH Lin. “Loihi: A Neuromorphic Manycore Processor with On-Chip Learning,” IEEE Micro / Intel Labs. 2018.
9. J Silva, AJER da Silva, RA Rodrigues. “Customizable FPGA-Based Hardware Accelerator for Convolutions and Deep Learning Primitives,” Sensors (MDPI). 2022.

10. W Lin, T Chen, V Sze. “Low-Power Ultra-Small Edge AI Accelerators for Image Classification,” Electronics (MDPI). 2021.
11. IEA-4E EDNA, “Energy Harvesting Technologies for IoT Edge Devices”-technical survey/report (IEA 4E), 2018-(energy-harvesting overview for IoT/edge)
12. M Potocny, Coauthors. “Low-Voltage DC-DC Converter and Power-Management Techniques for On-Chip Energy Harvesting in IoT,” Sensors (MDPI). 2021.
13. Q Xu, T Mytkowicz, NS Kim. “Approximate Computing — A Survey,” IEEE Design & Test (survey on approximation for energy efficiency). 2016.
14. A Basu. “Spiking Neural Network Integrated Circuits: A Review of Trends and Future Directions” (survey on SNN VLSI / neuromorphic ICs), arXiv. 2022.
15. A. Prasad / R. Prasad, “An ultra-low-power CGRA for accelerating transformers and edge AI workloads” (CGRA / edge accelerator design trends & low-power reconfigurable arrays)-recent architecture/design preprint.
16. PP Ray, B Chowhan, N Kumar, A Almogren. “BIoTHR: Electronic health record servicing scheme in IoT-blockchain ecosystem,” IEEE Internet of Things Journal. 2021. 8: 10857-10872.
17. B Chouhan, R Pai, B Pandey. “Edge computing based emulator design for low-latency IoT health monitoring system,” International Journal of Information Technology. 2025. 1-11.
18. B Chowhan, R Mandal, PK Sharma. “DengueCBC: Dengue EHR transmission using secure consortium blockchain-enabled platform,” in Data Management, Analytics and Innovation (ICDMAI 2020), vol. 1. Singapore: Springer. 2020. 87-106.
19. B Mulla, B Chouhan, B Pandey. “An edge-IoT system for continuous pulse monitoring in personal healthcare,” in Proc. 2025 IEEE Madhya Pradesh Section Conf. (MPCON). 2025. 858-863.
20. IJ Goodfellow. “Generative adversarial nets,” in Advances in Neural Information Processing Systems (NeurIPS). 2014. 27.
21. S Siddamsetty, BB Chavan, V Langaliya, B Pandey. “Designing cybersecurity ecosystems: Lessons from the Kyiv breach and the ECLIPSE economic model.
22. RR Pai, JP Pendyala. “Optimizing healthcare pipelines for patient benefit: A data engineering perspective on preauthorization delays and denials,” in Proc. Int. Conf. on Software Engineering and Data Engineering, Cham, Switzerland: Springer Nature. 2025. 40-52.
23. R Somayajula, RR Pai, N Sajanraj, K Shah. “Zero-ETL architectures for AI workloads: Direct ML model access on cloud-native OLAP systems,” in Proc. 2025 Int. Conf. on Computing Technologies (ICOCT), IEEE. 2025. 1-7.
24. K Alang, SB Peta, RR Pai, B Patil. “Scalable cloud architectures for efficient processing of multi-structured big data,” in Proc. 2025 Global Conf. in Emerging Technology (GINOTECH), IEEE. 2025. 1-6.
25. RR Pai, JP Pendyala. “End-to-end predictive analytics pipeline,” in Proc. Data Analytics and Management. 2025. 6: 370.
26. N Patel, H Chauhan, H Joshi. “Orchestrating intelligence: Governance and leadership frameworks for human-AGI collaboration in quantum systems,” in Interplay of Artificial General Intelligence with Quantum Computing: Towards Sustainability, Cham, Switzerland: Springer Nature Switzerland. 2025. 255-272.
27. M Rana, T Joshi, M Malik. "Enhancing Retail System Resilience Through Integrated Cloudless AI and AIOps: A Framework for Real-Time Market Adaptation and Consumer Behavior Response," 2025 IEEE International Conference on Artificial Intelligence in Engineering and Technology (IICAIET), Kota Kinabalu, Malaysia. 2025. 407-412.
28. M Rana, N Giri, M Malik. "DevSecPrivacyAIOps: An Integrated Framework for Intelligent Security, Privacy, and Operations in Modern Software Development," 2025 International Conference on Information Technology and Computing (ICITCOM), Yogyakarta, Indonesia. 2025. 439-444.
29. H Rehan, G Sunkara, V Sannamuri, M Malik, K Jayabalan, et al. "DeepShield: Privacy-Preserving Malware Classification using Split Learning," 2025 6th International Conference on Electronics and Sustainable Communication Systems (ICESC), Coimbatore, India. 2025. 1812-1819.
30. SR Singh, G Sakya, M Malik, C Grover. "Smart Agricultural BOT for Automated Seed Sowing and Soil Monitoring in Organic Farming," 2025 International Conference on Networks and Cryptology (NETCRYPT), New Delhi, India. 2025. 1732-1736.
31. M Rana, B Pandey, Eds. Quantum Ops: Bridging Quantum Computing and IT Operations. Cham, Switzerland: Springer. 2026.
32. B Pandey, A Patel, Eds. Revolutionizing the Cloud: Generative AI, Security, and Sustainability. Cham, Switzerland: Springer. 2026.
33. AR Ekkati, BK Pandey, Eds. AI-Powered Cybersecurity Essentials: Protecting Enterprise Networks. Cham, Switzerland: Springer. 2026.
34. V Gudur, B Pandey, A Patel, Eds. Trustworthy AI Systems: Engineering Secure, Scalable, and Responsible Intelligence for Real Applications. Cham, Switzerland: Springer. 2026.